Architecture and Design of the AGIPD Detector for the European XFEL

J. Becker, L. Bianco, P. Göttlicher, H. Graafsma*, H. Hirsemann, S. Jack, A. Klyuev, A. Marras, , U. Trunk (DESY, Hamburg, Germany)
R. Klanner, J. Schwandt, J. Zhang (University of Hamburg, Germany)
R. Dinapoli, D. Greiffenberg, B. Henrich, A. Mozzanica, B. Schmitt, X. Shi (PSI, Villigen, Switzerland)
M. Gronewald, H. Krüger (University of Bonn, Germany)

***Abstract*—AGIPD is a hybrid pixel detector developed by DESY, PSI, the University of Bonn and the University of Hamburg. The detector is targeted for use at the European XFEL, a source with unique properties: a bunch train of 2700 pulses with $> 10^{12}$ photons of 12 keV each, only 100 fs long and with a 220 ns spacing, is repeated at a 10 Hz rate. This puts up very demanding requirements: dynamic range has to cover the detection of single photons and extend up to $> 10^4$ photons/pixel in the same image, and as many images, as possible have to be recorded in the pixel to be read out between pulse trains. The high photon flux impinging on the detector also calls for a very radiation hard design of sensor and ASIC. The detector will consist of 16 Sensor modules arranged around a central hole for the direct beam. Each made of a single sensor bump-bonded to 2×8 readout chips of 64×64 pixels in a grid of 200 µm pitch. Each pixel of these ASICs contains a charge sensitive preamplifier featuring adaptive gain switching, changing sensitivity in three ranges, and a buffer to provide correlated double sampling (in the highest sensitivity mode). Most of the pixel area, albeit, is used for an analogue memory to record 352 frames. It is operated in random-access mode: data containing bad frames can be overwritten and the memory can be used in the most efficient way. The readout between two bunch trains is arranged via 4 ports: Data from pixels of one row is read in parallel and serialised by 4 multiplexers at the end of the pixel columns and driven off-chip as differential signals. The operation of the ASIC is controlled via a three-line serial interface, using a command based protocol. It is also used to configure the chip's operational parameters and internal timings.**

***Index Terms*—XFEL, 2D detector, Hybrid Pixel Detector.**

I. European XFEL challenges

THE European X-Ray Free Electron Laser (XFEL) under construction in Hamburg will provide fully coherent, $<$ 100 fs long X-ray pulses, with up to 10^{12} photons at 12 keV. The high intensity per pulse will allow recording diffraction patterns of single macromolecules or small crystals in a single shot. As a consequence the 2D detectors have to cope with a large dynamic range in the images, ranging from a single photon to $> 10^4$ photons/pixel. An additional challenge is the European XFEL time structure (c.f. fig. 1): an electron bunch train with 10 Hz repetition rate, consisting of up to 2,700 bunches with a 220 ns spacing. Thus the recorded images have to be stored for every pixel during the bunch trains and read out between bunch trains. AGIPD is one of 3 detector development projects supported by the European XFEL to cope with these requirements.

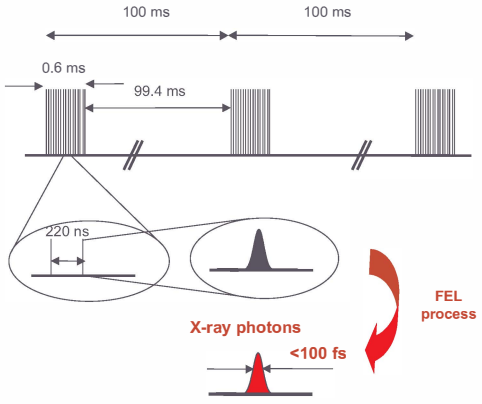

Fig. 1. Time structure of the European XFEL

A. Detector challenges

Time structure of the photon signals calls for a pipelined architecture: recording 2,700 frames of a bunch train at a rate of 4.5 Mhz and the delayed readout of this data from a detector within the 99.4 ms bunch gap in an ideal case. However, the integration density of current CMOS technologies, the required sensitivity to single photons and the expected radiation dose, together with the chosen pixel size of 200 µm $\times$ 200 µm limit the storage depth of an analogue memory to 352 images, i.e. 352 samples per pixel. To optimise the use of this limited storage depth, the memory is operated in random access mode. This way empty or bad images (i.e. when the X-ray pulse did not hit the target in case of single molecule imaging) can be overwritten with meaningful data, when this information becomes available from diagnostic detectors (e.g. registering fluorescent light) microseconds later.

Also the large dynamic range of the expected signals is very demanding: while single photons of 12 keV have to be detected with sufficient noise margin, the highest expected signals are up to $\gtrapprox 10^4$ photons per pixel in the same image. To provide this dynamic range with a sufficient S/N ratio, the sensitivity

* also Midsweden University, Sundsvall, Sweden

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U. Trunk is with Deutsches Elektronen-Synchrotron DESY, D-22603 Hamburg, Germany. e-mail: ulrich.trunk@desy.de.

of the preamplifier is dynamically adapted to the incoming signal.

Such high signals also provide a challenge for the sensor itself, since 10^5 photons in 10µm × 10µm will create $10^5 \times 12 \cdot 10^3)/3.6 = 3 \times 10^8$ electron-hole pairs at 12 keV. The high charge carrier density will effectively shield the field inside the sensor. The charge cloud has to spread in space (and time) allow the depletion field to become dominant again for charge collection. Results of the extensive studies on this subject for the development of AGIPD are published in [8].

These high intensities will also result in a substantial accumulated dose: over three years the example above would result in 1 GGy impinging the sensor, while the ASIC underneath would still accumulate $> 10\mathrm{MGy}$. Thus investigations on radiation damage on sensors [9] and on the radiation hardness of the electronics are performed. Despite the use of radiation hard layout techniques, many circuit components, especially the capacitors and switches (FETs) of the analogue memory, are deemed critical.

II. AGIPD

A. Basic Parameters

AGIPD [2] [3] [6] is a flat $1\mathrm{k} \times 1\mathrm{k}$ hybrid pixel detector featuring a pitch of 200 µm, composed of 2×8 sensor modules of $512 \times 128 = 65536$pixels (with double sized pixels horizontally in between ASICs), as fig. 2 shows. The surface of each sensor is $105.2 \times 25.8\,\mathrm{mm}^2$ and does not have any gaps or other dead area. The sensors are bump-bonded to 2×8 readout ASICS to form a module. Four of these modules are mounted to a cooling plate to form a quadrant.

B. Detector mechanics

The four quadrants are movable inside a secondary vacuum and are shifted with respect to each other to form a hole for the very intense direct beam to pass (c.f. fig. 3). A beam stop in front of the detector or a gas-filled flight tube would cause a background exceeding the actual signal by several orders of magnitude.

For certain types of experiments the option for a second detector plane of 1024×128 pixels is planned. It will be mounted downstream of the main detector plane and will consist of two sensor modules, mounted with a small gap in between, once again for the direct beam to pass.

III. Readout ASIC

Each readout chip contains a square matrix of 64×64 pixels, read out on four ports. Each pixel contains

- a charge sensitive preamplifier
- a discriminator
- the switch control circuit and a DAC to encode the switch settings
- a CDS[1] buffer
- analogue memory of 2×352 cells
- a charge sensitive readout buffer.

[1] correlated double sampling – Samples are only correlated for the highest sensitivity. The correlation is broken if gain switching occurs.

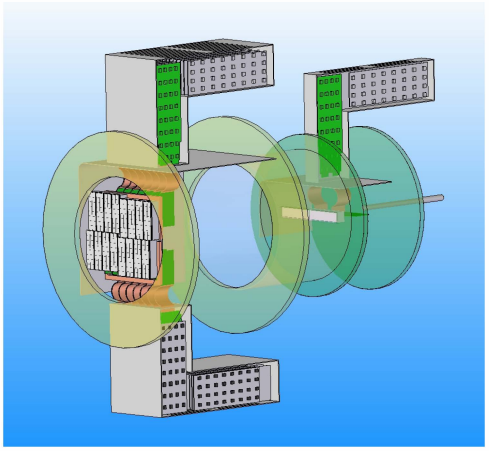


Fig. 3. Sketch of the mechanical layout of the AGIPD detector.

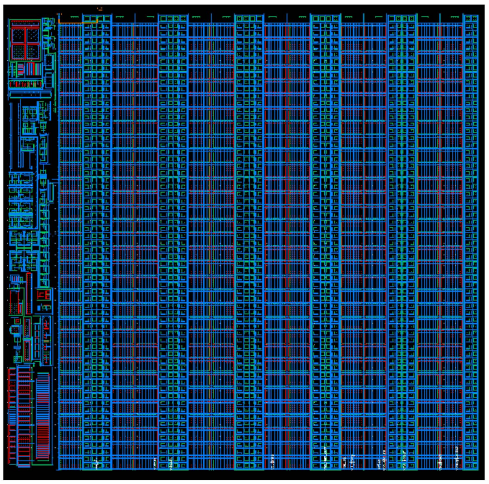


Fig. 5. Layout of a pixel of AGIPD 0.4 (and 1.0). Only the narrow stripe on the left hand side contains active circuitry, most of the area is occupied by the analogue memory

These buffers connect to one of the two readout buses per pixel column, which serve the pixels of even and odd rows respectively. The pixel matrix is subdivided in 4 blocks of 16×64 pixels, operating in parallel. Each of these blocks connects to a multiplexer and output buffer. The command based control of the chip is based on a 3-line serial interface. The block schematic of the ASIC is depicted in fig. 4, while fig. 5 shows the layout of a single pixel.

A. Architecture

The output of the charge sensitive preamplifier not only connects to the CDS buffer, but also to a discriminator. If an input signal triggers this discriminator, additional feedback capacitors are added to the preamplifier feedback, thus lowering sensitivity and increasing the dynamic range in two steps. The output of the CDS buffer and an analogue encoding of the selected gain are written to the analogue memory, which can store 352 samples.

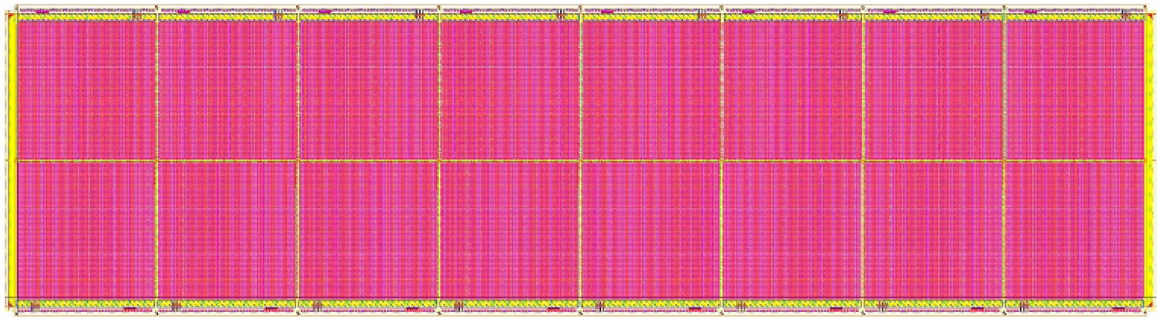


Fig. 2. Drawing of an AGIPD sensor module, consisting of the silicon sensor itself and 2 × 8AGIPD ASICs bump-bonded to it.

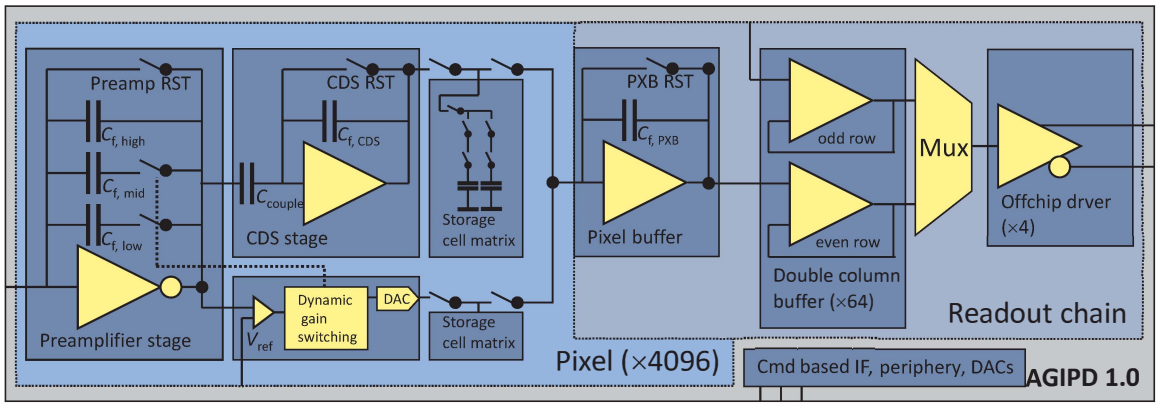


Fig. 4. Schematic of the AGIPD 1.0 readout ASIC

B. Adaptive gain switching

The preamplifier uses a simple inverter as a core cell. Feedback is provided by means of a 60 fF MiMCap[2]. For lower sensitivities, additional dual-MiMCaps of 3 pF and 10 pF respectively are connected in parallel to the initial feedback. Delays in the control circuitry of the gain switching ensure proper operation in case of the instantaneous signal of an FEL.

C. Embedded analogue memory

The analogue memory consists of two types of storage cells: for amplitude values ($C_{\mathrm{store}} \approx 200$fF) and for the encoded gain settings ($C_{\mathrm{store}} \approx 30$fF), as fig 6 shows.

The requirements on amplitude values are demanding an accuracy of better than 0.1 photon to ensure the single photon sensitivity of the detector, which translates to 0.1% of the preamplifier-CDS frontend output range, maintained for a storage time of at least 10 ms. Thus leakage currents in the storage capacitors and switches were considered the most critical issue in the ASIC design and investigated with the very first chips submitted (HPAD 0.1 and HPAD 0.2). These storage cells are also considered the part of the circuit most seriously affected by radiation damage, which was also investigated with these chips. As a result storage cells use a DGNCAP[3] as storage element and two thin-oxide p-FETs as switches (c.f. fig. 7). The two transistors in series serve two purposes:

[2]Metal-inter-metal capacitor, formed by a thin dielectric and an additional metal layer in the BEOL.

[3]Thick oxide n-FET in an n-well

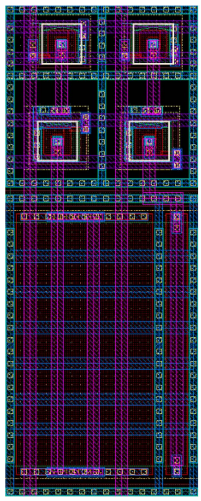


Fig. 6. Layout of the storage cells in the analogue memory of AGIPD: The big capacitor on the left hand side is used to store the signal amplitude, while the small on on the right hand side stores the preamplifier gain, encoded to three analogue levels.

- A logic AND of the row and column lines of the Memory is formed.
- The voltage drop across the lower FET and thus the leakage current is minimised.

For the capacitor a DGNCAP was used, since these devices are radiation hard and show no measurable leakage due to the thick dielectric layer employed.

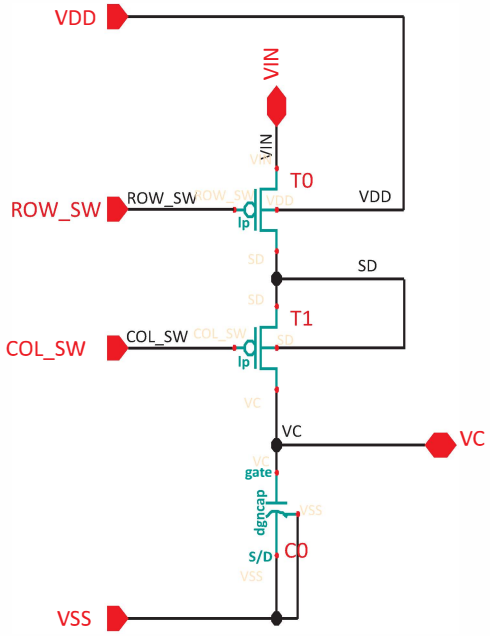


Fig. 7. Schematic of the storage cells in the analogue memory of AGIPD.

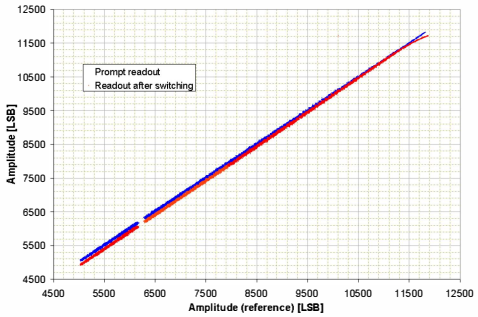


Fig. 9. Impact of memory access (switching) on the stored signals (on AGIPD 0.3). The data of the red dots are read out without any prior switch operation. For the blue dots the column switch was operated 70, the row switch 32 times before readout. The "gaps" of the curves are caused by data loss due to a disk failure.

D. Radiation hardness

Extensive studies on the radiation hardness of the storage cells have been performed with several prototype chips. While the floating n-well ensured a very low leakage for non-irradiated chips, surface charges caused an inversion layer around this n-well after $\leq 100\text{kGy}$. This layer substantially increases the area for the collection of minority carriers (i.e. electrons), leading to a rapid discharge of the n-well. In turn the pn-junction inside the n-well is forward biased, and the capacitor is discharged. To circumvent this behaviour, a diffusion ring, biased to a positive voltage was placed around the floating n-well. It serves to collect the minority carriers, directly or via the radiation-induced inversion layer. If the inversion grows stronger, i.e. turns into a parasitic channel, it pulls up the n-well to a positive potential. Albeit this sacrifices the zero voltage drop across the switch for higher doses, it reliably prevents the discharge of the storage cells due to a forward biased pn-junction.

These radiation hardness studies furthermore showed, that cooling a chip dosed with 100 kGy to $-20°\text{C}$ restored its non-irradiated droop behaviour. It also turned out, that LP[4]-FETs, which due to the higher V_{th} show a lower initial leakage current, degrade more with dose than their RVT[5]-counterparts, which in turn were used for the switches.

E. Readout sequence

The access switches of the pipeline form a logic "AND", which is exploited as part of the memory addressing scheme, and could cause an additional charge loss. However, the foreseen readout sequence of AGIPD, illustrated in fig. 8, operates the switches in a non-interleaved fashion:

The worst case is the last memory cell in the bottom pixel row, its column switch is operated $(64 \times 11) - 1 = 703$ times and the row switch $32 - 1 = 31$ times (due to column parallel readout), before the cell is finally read. Nevertheless, due to the non-interleaved operation of the switches, only the charge on the node between the two switches is lost, as fig. 9 shows.

F. Periphery & serial interface

The command based interface uses three lines (fig. 10): clock, data and *start of bunch*. The latter triggers the interpretation of a command, i.e. its execution. Thus it also provides the synchronisation with the European XFEL's 4.5 MHz bunch timing. Since the command length is 16 bits, the clock signal has to be at least 72 MHz for sampling and 7.6 MHz to accomplish the readout of $352 \times 2 \times 16 \times 64$ samples within 99.4 ms. This clock signal also serves as an internal timing reference, i.e. determines the granularity of all internal signals, like preamp reset time and the CDS integration period, since these are derived from it by means of a programmable sequencer, as shown in fig. 11. At the European XFEL it is planned to operate AGIPD with a 99 MHz clock. Thus the sequence to capture a frame is 22 clock cycles, while readout at 33 MHz is envisaged, since the readout multiplexer uses a programmable clock divider.

The *Periphery* also implements the random access to the memory and the control of the interleaved column parallel readout (fig. 12): The cells of a defined memory address are read out for one pixel row and driven down one of the column buses, while the signals of the previous row are still connected to the other column bus, are serialised and driven off chip via multiplexer and off-chip driver. This way the pixel readout buffer can be much slower and less power consuming. Only the multiplexer and the readout buffer operate at the full readout speed.

The implementation of the interface on AGIPD 1.0 will implement 6 types of commands:

- Capture frame (argument: memory address)
- Set memory address (argument: memory address), it can also serve as a NOP[6] command
- Program the status register (argument: register bits)

[4]Low-power (high) V_{th}
[5]Regular V_{th}
[6]no operation

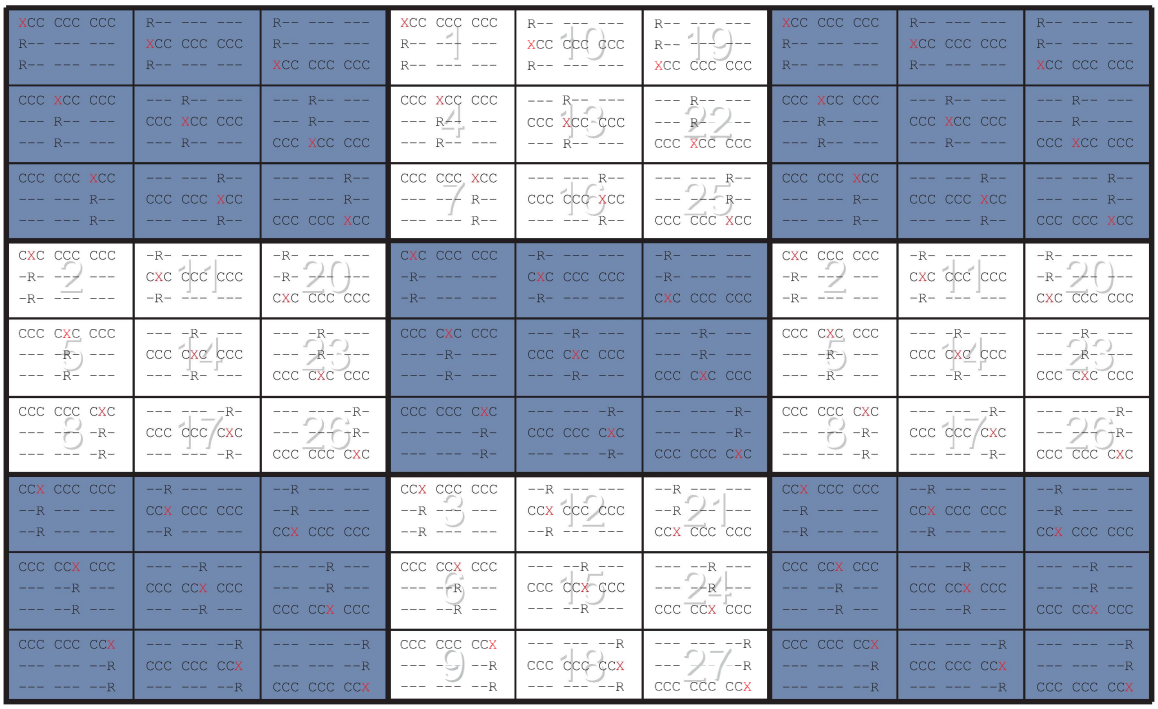


Fig. 8. Switching sequence of pixels and memory cells on AGIPD. The scheme only shows 3 × 3 pixels with 3 × 3 storage cells. C indicates the column switch and R the row switch being closed, X indicates the readout of the memory cell (i.e. both switches are closed).

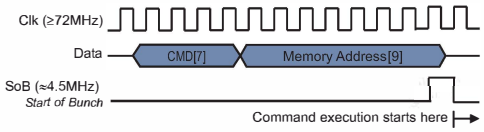


Fig. 10. Data format of AGIPD 1.0's control interface.

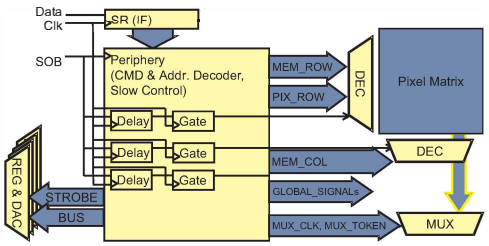


Fig. 11. Block schematic of the interface and control circuit of AGIPD 1.0.

- Program internal timings (arguments: function, time in clock cycles)
- Program on-chip DACs/registers (arguments: DAC/register address, DAC/register value)
- Read pixel (arguments: read mode[7], prefetch pixel row, mux pixel row)

IV. Prototyping

For the development of the AGIPD readout ASIC, several prototypes and test chips have been produced. In addition to the readout chips listed in tab. I, two chips, HPAD 0.1 and HPAD 0.2, have been manufactured to evaluate the radiation hardness of the chosen 130 nm CMOS technology and its components.

[7]3 bits encoding analogue/$\overline{\text{gain}}$ readout, first row, last row

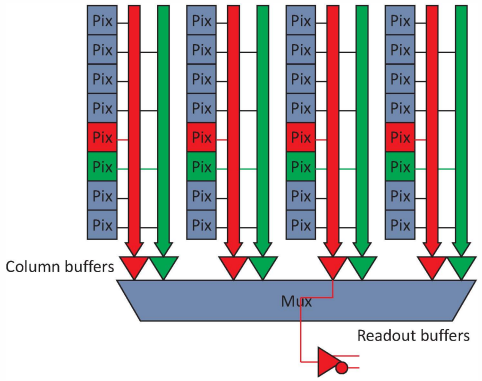


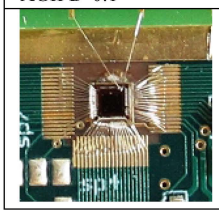
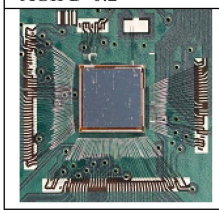
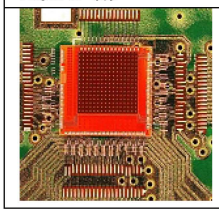
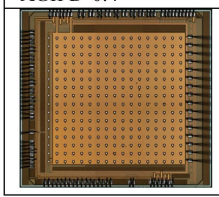
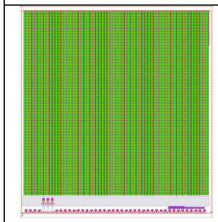
Fig. 12. Visualisation of AGIPD 1.0's column parallel readout scheme.

V. Status & Outlook

AGIPD is a hybrid pixel detector for the European XFEL with 1024 × 1024 Si-pixels of $(200\,\mu\text{m})^2$ size. It provides single photon sensitivity and a $> 10^4$ photons dynamic range at 12 keV by means of adaptive gain switching. It features random access to an analogue storage for 352 images, thus enabling veto and trigger capabilities. Images are recorded at 4.5 MHz frame rate at the European XFEL, while readout will use 33 MHz. A radiation hard design for $\gg$ 10MGy on the ASIC has been employed.

Currently a fully functional 16 × 16 pixel prototype readout chips, AGIPD 0.2, 0.3, 0.4 are available, while a full sized (64 × 64 pixel) readout chip is planned for 2012. Single

TABLE I
LIST OF AGIPD (PROTOTYPE) ASIC SUBMISSIONS. THE RIGHTHAND COLUMN LISTS THE FEATURES OF THAT CHIP AND THE SUBCIRCUITS UNDER TEST.

AGIPD 0.1	Jan. 2009
	• No pixels • 3 readout blocks consisting of: – Readout chain (Preamp + CDS stage) – 3 different kinds of leakage current compensation
AGIPD 0.2	May 2009
	• 16×16 pixels • 100 storage cells • No leakage current compensation • Different combinations of preamps and storage cell architectures
AGIPD 0.3	Nov. 2010
	• 16×16 pixels • 200 storage cells • Radiation hard storage cell design • High speed command based control interface • Improved discriminator and CDS buffer
AGIPD 0.4	Nov. 2011
	• 16×16 pixels • High sensitivity preamp ($C_\mathrm{f} = 60\,\mathrm{fF}$) • 352 storage cells • Double-column readout • New multiplexer • New off-chip buffer • No command based control circuit
AGIPD 1.0	Q4 2012
	Full-scale chip: • 64×64 pixels • High sensitivity preamp ($C_\mathrm{f} = 60\,\mathrm{fF}$) • 352 storage cells • Double-column readout • High speed command based control interface

2×8-chip detector modules are expected for 2013, while the 1 megapixel detector system is expected to be available 2014.

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